AMENDMENT TO THE SPECIFICATION

Please replace the paragraph beginning on line 6 of page 1 with the following replacement paragraph:

This application is a continuation-in-part of U.S. Pat. Appl. Ser. No. 10/761,022 filed on January 20, 2004 and entitled "Multi-Terminal Devices having Logic Functionality", which is a continuation in part of U.S. Pat. Appl. Ser. No. 10/657,285 filed on September 8, 2003 and entitled "Multiple Bit Chalcogenide Storage Device", which is a continuation-in-part of U.S. Pat. No. 6,969,867, ~~Appl. Ser. No. 10/426,321 filed on April 30, 2003 and~~ entitled "Field Effect Chalcogenide Devices", which is a continuation-in-part of U.S. Pat. No. 6,967,344, ~~Appl. Ser. No. 10/384,994 filed on March 10, 2003 and~~ entitled "Multi-Terminal Chalcogenide Switching Devices", the disclosures of which are hereby incorporated by reference herein.

Please replace the paragraph beginning on line 15 of page 3 with the following replacement paragraph:

One of the instant inventors, S.R. Ovshinsky, has recently proposed new uses of chalcogenide phase-change materials as active materials for the processing and storage of data. In U.S. Pat. No. 6,671,710 (the '710 patent), the disclosure of which is hereby incorporated by reference herein, Ovshinsky et al. describe a principle of operation of phase-change materials in conventional and cognitive computing applications. Phase-change materials can not only operate in the binary mode characteristic of conventional silicon computers, but also offer opportunities for the non-binary storage and processing of data. Non-binary storage provides for high information-storage densities, while non-binary processing provides for increased parallelism of

operation. The '710 patent also describes representative algorithms that utilize a non-binary computing medium for mathematical operations such as addition, subtraction, multiplication and division. U.S. Pat. No. 6,714,954 (the '954 patent) ~~Appl. Ser. No. 10/155,527 (the '527 application)~~ by Ovshinsky et al., the disclosure of which is hereby incorporated by reference herein, describes further mathematical operations based on a phase-change computing medium, including factoring, modular arithmetic and parallel operation.

Please replace the paragraph beginning on line 5 of page 4 with the following replacement paragraph:

In U.S. Pat. No. 6,999,953 (the '953 patent) ~~Appl. Ser. No. 10/189,749 (the '749 application)~~, the disclosure of which is hereby incorporated by reference herein, Ovshinsky considers the architecture of computing systems based on devices utilizing a phase-change material as the active computing medium. More specifically, Ovshinsky considers networks of phase-change computing devices and demonstrates functionality that closely parallels that of biological neural networks. Important features of this functionality include the accumulative response of phase-change computing devices to input signals from a variety of sources, an ability to weight the input signals and a stable, reproducible material transformation that mimics the firing of a biological neuron. This functionality enables a new concept in intelligent computing that features learning, adaptability, and plasticity.

Please replace the paragraph beginning on line 15 of page 4 with the following replacement paragraph:

In U.S. Pat. Nos. 9,967,433 ('344 patent) and 6,969,867 ('867 patent) and U.S. Pat. Appl. Ser. Nos. ~~10/384,994 (the '994 application); 10/426,321 (the '321 application);~~ 10/657,285 (the '285 application), and 10/761,022 (the '022 application), ~~,~~ the disclosures of which are hereby incorporated by reference herein, Ovshinsky et al. further develop the notion of phase-change computing by discussing additional computing and storage devices. The '344 patent ~~'994 application~~ discusses a multi-terminal phase-change device where a control signal provided at one electrical terminal modulates the current, threshold voltage or signal transmitted between other electrical terminals through the injection of charge carriers. The '867 patent ~~'321 application~~ describes a related multi-terminal device that utilizes a field effect terminal to modulate the current, threshold voltage or signal transmitted between other terminals. The devices described in the '344 and '867 patents ~~'994 and '321 applications~~ may be configured to provide a functionality analogous to that of the transistor that is so vital to silicon based computers. The '285 application presents multiple-bit storage devices having multiple terminals that utilizes a phase-change material. The '022 application describes multi-terminal logic devices that utilize a phase-change material.

Please replace the paragraph beginning on line 16 of page 7 with the following replacement paragraph:

The registers included in an embodiment of the instant secured devices have been previously described in the '710, '954, and '953 patents ~~patent and in the '527, and '749 applications~~ and include two-terminal phase-change devices. The weighting devices have been

previously described in the '953 patent ~~'749 application~~ and include two-terminal phase-change devices. The registers store and/or process information through manipulations of the structural state of a phase-change material according to one mechanism. The weighting devices resistively modify the transmission of electrical signals passing through themselves by manipulations of the structural state of a phase-change material according to a second mechanism. The mechanisms of structural variations are described in more detail hereinbelow.

Please replace the paragraph beginning on line 3 of page 8 with the following replacement paragraph:

As described hereinabove, the registers and weighting devices that may be used as phase-change elements in the instant secured devices include two-terminal phase-change devices such as those described or incorporated by reference in the '710, '954, and '953 patents ~~patent and '527 and '749 applications~~. Among those devices are the two-terminal devices discussed in U.S. Pat. Nos. 5,714,768, 5,912,839 and 6,141,241, the disclosures of which are hereby incorporated by reference. These patents include a description of device structures, materials, growth methods, layer thicknesses etc. A representative two-terminal device that may be used as a register or weighting device is shown in Fig. 1. The device includes a substrate **2** (e.g. Si), lower electrical contact **5** (e.g. carbon, a metal or metal alloy, typical thickness of a few to several hundred angstroms (e.g. 600 Å)), insulating layer **15** (e.g. SiN_x, SiO_2, typical thickness of a few to several hundred angstroms (e.g. 800 Å)), phase-change material **25** (having typical layer thickness outside of central pore of a few to several hundred angstroms (e.g. 600 Å)), and upper electrical contact **35** (e.g. carbon, a metal or metal alloy, typical thickness of several hundred to a few thousand angstroms (e.g. 2000 Å)). Further details concerning materials and dimensions for

electrical terminals or contacts, insulating materials, and other layers are similar to those previously described in the '344, and '867 patents and in the ~~'994, '321~~ '285 and '022 applications.

Please replace the paragraph beginning on line 14 of page 13 with the following replacement paragraph:

The resistance plot includes two characteristic response regimes of a chalcogenide material to electrical energy. The regimes are approximately demarcated with the vertical dashed line **10** shown in Fig. 2. The regime to the left of the line **10** may be referred to as the accumulating regime of the chalcogenide material. The accumulation regime is distinguished by a nearly constant or gradually varying electrical resistance with increasing electrical energy that culminates in an abrupt decrease in resistance at and beyond a threshold energy. The accumulation regime thus extends, in the direction of increasing energy, from the leftmost point **20** of the resistance plot, through a plateau region (generally depicted by **30**) corresponding to the range of points over which the resistance variation is small or gradual to the set point or state **40** that follows an abrupt decrease in electrical resistance. The plateau **30** may be horizontal or sloping. The left side of the resistance plot is referred to as the accumulating regime because the structural state of the chalcogenide material continuously evolves as energy is applied, with the fractional crystallinity of the structural state correlating with the total accumulation of applied energy. The leftmost point **20** corresponds to the structural state in the accumulating regime having the lowest fractional crystallinity and may be referred to as the reset state. This state may be fully amorphous or may contain some residual crystalline content. As energy is added, the fractional crystallinity increases, and the chalcogenide material transforms in the direction of

increasing applied energy among a plurality of partially-crystalline states along the plateau **30**. Selected accumulation states (structural states in the accumulation region) are marked with squares in Fig. 2. Upon accumulation of a threshold amount of applied energy, the fractional crystallinity of the chalcogenide material increases sufficiently to effect a setting transformation characterized by a dramatic decrease in electrical resistance and stabilization of the set state **40**. The structural states in the accumulation regime may be referred to as accumulation states of the chalcogenide material. Structural transformations in the accumulating regime are unidirectional in the sense that they progress in the direction of increasing applied energy within the plateau region **30** and are reversible only by first driving the chalcogenide material through the set point **40** and resetting as described in, for example, the <u>'954 and '953 patents</u> ~~'527 and '749 applications~~.

Please replace the paragraph beginning on line 18 of page 14 with the following replacement paragraph:

While not wishing to be bound by theory, the instant inventors believe that the addition of energy to a chalcogenide material in the accumulating regime leads to an increase in fractional crystallinity through the nucleation of new crystalline domains, growth of existing crystalline domains or a combination thereof. It is believed that the electrical resistance varies only gradually along the plateau **30** despite the increase in fractional crystallinity because the crystalline domains form or grow in relative isolation of each other so as to prevent the formation of a contiguous crystalline network that spans the chalcogenide material. This type of crystallization may be referred to as sub-percolation crystallization. The setting transformation coincides with a percolation threshold in which a contiguous, interconnected crystalline network

forms within the chalcogenide material. Such a network may form, for example, when crystalline domains increase sufficiently in size to impinge upon neighboring domains. Since the crystalline phase of chalcogenide materials is more conductive and less resistive than the amorphous phase, the percolation threshold corresponds to the formation of a contiguous low resistance conductive pathway through the chalcogenide material. As a result, the percolation threshold is marked by a dramatic decrease in the resistance of the chalcogenide material. The leftmost point of the accumulation regime may be an amorphous state or a partially-crystalline state lacking a contiguous crystalline network. Sub-percolation crystallization commences with an initial amorphous or partially-crystalline state and progresses through a plurality of partially-crystalline states having increasingly higher fractional crystallinities until the percolation threshold is reached and the setting transformation occurs. Further discussion of the behavior of chalcogenide materials in the accumulation regime is provided in the '867, '954, and '953 patents ~~'319, '527, and '749 applications~~ and in U.S. Pat. Nos. 5,912,839 and 6,141,241; the disclosures of which are hereby incorporated by reference herein.

Please replace the paragraph beginning on line 12 of page 17 with the following replacement paragraph:

Chalcogenide phase-change devices in accordance with the instant secured devices include those that operate in either or both of the accumulation or greyscale regimes of the resistance plot. The '710, '954, and '953 patents ~~patent and the '527 and '749 applications~~ describe cognitive registers that operate in the accumulation regime between the reset state **20** and set state **40**, inclusive. These cognitive registers may be used to store or process data or information in a binary or non-binary fashion or to encrypt data or information. Cognitive registers may thus

be used as encryption devices as described in the '710 patent. The '953 patent ~~'749 application~~ describes weighting devices that operate in the grayscale region between the set state **40** and reset state **60**, inclusive. The weighting devices resistively modify signals transmitted between circuit elements connected thereto so that the level or magnitude of the signal transmitted from one circuit element to another may be modulated or otherwise varied by controlling the resistive state of the weighting device. The current passing through a weighting device is modified via the resistance or resistive state of the weighting device. In a preferred embodiment, a weighting device has two or more resistance states, each of which is distinguished by a different resistance value. The weighting devices may be used, for example, as interconnection devices in circuits or to weight input signals provided to a circuit element, including nodes of neural networks or the cognitive registers described hereinabove. The resistance of a weighting device may possess interpretative significance (e.g. in neural network applications the resistance corresponds to a weighting factor which may be viewed as a form of memory with respect to neural processing; information may also be encoded through the resistance of a weighting device), and it may thus be desirable to protect it via the secured device of the instant invention.

Please replace the paragraph beginning on line 22 of page 18 with the following replacement paragraph:

The instant secured devices combine a security element with a phase-change device such as a register or weighting device. The security element is a three-terminal device that is combined in parallel with a register or weighting device to provide a secured device according to the instant invention. The security element may be a conventional silicon based transistor or a three-terminal phase-change device such as those described in the '344 and '867 patents ~~'994~~

~~and '321 applications~~. A schematic depiction of a secured device according to the instant invention is provided in Fig. 3. The device includes a parallel combination **105** having a security element **110** and a phase-change element **120**. Control systems **130** and **140** for the security element **110** and phase-change element **120**, respectively, are also included. The phase-change element **120** may be a register or weighting device and includes a phase-change material as the working substance. In a preferred embodiment, the phase-change material is a chalcogenide such as those described hereinabove. The phase-change element may utilize accumulation states, grayscale states or a combination thereof in its operation as a processing or storage element.

Please replace the paragraph beginning on line 12 of page 19 with the following replacement paragraph:

The security element **110** includes three terminals, **112**, **114** and **116**. Terminals **112** and **114** are used to establish parallel connectivity of the security element **110** with the phase-change device **120** as shown in Fig. 3. Terminal **116** is connected to controlling electronics **130** that are used to control the state of the security element **110**. More specifically, a control signal provided from control system **130** may be used to regulate the current flow or resistance between terminals **112** and **114** of the security element. In an embodiment in which the security element **110** is a transistor, for example, terminal **116** may be a gate terminal that regulates the current flow between terminals **112** and **114** that function respectively as base and emitter terminals (or vice versa). In an embodiment in which the security element **110** is a three-terminal chalcogenide device, terminal **116** may be a control terminal that modulates the current flow or resistance between terminals **112** and **114**. As described in the <u>'344 and '867 patents</u> ~~'994 and '321 applications~~, the control terminal of a multi-terminal chalcogenide device may influence current

flow, filament formation or resistance through, for example, the direct injection of carriers or via a field effect.

Please replace the paragraph beginning on line 16 of page 27 with the following replacement paragraph:

Similar considerations pertain to the use of a three-terminal phase-change device as a security element of the instant invention. As described in the '344 and '867 patents ~~'994 and '321 applications~~, three-terminal phase-change devices utilize a control terminal to regulate the current flowing between two other (non-control) terminals of the device. The non-control terminals are used to establish parallel connectivity with the phase-change element of the instant invention. A signal applied to a control terminal may increase or decrease the current flowing between the non-control terminals and may do so through a current-injection mechanism or a field-effect mechanism. An increase in current flow corresponds to a decrease in the resistance of the phase-change material between the terminals through which the current flows and vice versa. In the context of the instant invention, the ON state of a three-terminal phase-change device is a state in which the control signal facilitates current flow through current injection of a field effect mechanism that lowers the resistance to current flow between a pair of terminals. Similarly, the OFF state of a three-terminal phase-change device is a state in which the control signal inhibits or prevents current flow between a pair of terminals. Since the range of control signals is continuously variable, a continuous range of resistances between two non-control terminals is available and may be used in the context of the instant invention. Resistances that are larger than, comparable to or smaller than the resistance of the phase-change element of the instant invention are available.